Electronic Version
Stylesheet Version v1.1.1

Description

MEHTOD OF MAKING A BIT LINE CONTACT DEVICE

BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention generally relates to semiconductor processes, and more particularly to a method for fabricating a bit line contact between two adjacent gate conductor stacks by utilizing a sacrificial polysilicon layer and spin-on glass (SOG) during the fabrication of a Trench-DRAM device.

[0003] 2. Description of the Prior Art

[0004] A memory chip is an integrated circuit (IC) made of millions of transistors and capacitors. In the most common form of computer memory, dynamic random access memory (DRAM), a MOS transistor and a storage capacitor are paired to create a memory cell, which represents a single bit of data. Memory cells are etched onto a silicon wafer in

an array of columns (bit lines) and rows (word lines). The intersection of a bitline and wordline constitutes the address of the memory cell. The storage capacitor holds the bit of information. The MOS transistor acts as a switch that lets the control circuitry on the memory chip read the storage capacitor or change its state. The storage capacitor typically comprises a top electrode, a storage node, and a capacitor dielectric layer. As DRAMs are manufactured with increasing densities, the memory cells necessarily are made smaller and smaller and packed closer and closer together to pack as much memory into as small a space as possible. The increased density drives the word lines (or bit lines) closer together increasing the coupling between adjacent lines and also challenges the conventional lithographic methods for transferring tiny feature images such as a bit line contact pattern.

[0005] Fig.1 to Fig.5 are schematic cross-sectional diagrams illustrating a conventional method for fabricating a bit line contact between two adjacent gate conductor stacks 12 and 14. As shown in Fig.1, on a main surface 11 of a semiconductor substrate 10, at least two gate conductor stacks 12 and 14 are provided. Each of the gate conductor stacks 12 and 14 generally comprises a gate dielectric

layer 22, a conductive layer 24 and a silicon nitride cap layer 26. A bit line contact area 42 and a non-bit line contact area 44 are defined over the gate conductor stacks 12 and 14. The bit line contact area 42 is approximately above the area between the gate conductor stacks 12 and 14. Typically, after the formation of the gate conductor stacks 12 and 14, a silicon nitride liner 32 is deposited on the semiconductor substrate 10. A borophosphosilicate glass (BPSG) layer 36 is then deposited on the silicon nitride liner 32.

[0006] As shown in Fig.2, a chemical mechanical polishing (CMP) process is then carried out to polish the BPSG layer 36 to the silicon nitride liner 32. As shown in Fig.3, a TEOS-oxide layer 38 is deposited on the remaining BPSG layer 36 and on the exposed silicon nitride liner 32. A photoresist pattern 52 is then formed on the TEOS-oxide layer 38 by using conventional lithographic methods. The photoresist pattern 52 has an opening 54 exposing the bit line contact area 42 between the gate conductor stacks 12 and 14.

[0007] As shown in Fig.4, using the photoresist pattern 52 as an etching hard mask, an anisotropic etching process is performed to etch the TEOS-oxide layer 38, the BPSG layer 36

and the silicon nitride liner 32 through the opening 54, thereby forming a bit line contact hole 62. Simultaneously, a silicon nitride spacer 64 is formed on sidewall of the gate conductor stacks 12 and 14. The photoresist pattern 52 is then removed.

[0008] Finally, as shown in Fig.5, the bit line contact hole 62 is filled with conductive materials such as metals or the like to form a bit line contact plug 64. Generally, the resultant bit line contact plug 64 is about 8000-angstrom height from the main surface 11 of the semiconductor substrate 10. The TEOS-oxide layer 38 has a thickness of about 3000 angstroms.

[0009] However, the above-described prior art method has several drawbacks. First, since the shrinkage of the bit line contact area 42, precise and accurate pattern transfer using conventional lithographic methods becomes a major challenge. As the bit line contact area 42 shrinks to below 90nm, it often needs so-called Imaging Enhancement Technology (IET) to successfully transfer such small bit line contact pattern from a photo mask to a photoresist layer on a wafer. The process window is therefore narrowed. Further, it is difficult to clean up a bit line contact hole having a depth of about 8000 angstroms and a criti-

cal dimension of about 90nm by using dry or wet etching methods. Some undesired residuals might clog the bit line contact hole. Another shortcoming is that the above-described prior art method uses silicon nitride liner 32. A part of the silicon nitride liner 32 is etched into a silicon nitride spacer 64 on sidewall of the gate conductor stacks 12 and 14. In operation, the silicon nitride spacer 64 leads to higher parasitic capacitance, which adversely affects the performance of the memory device.

SUMMARY OF INVENTION

[0010] Accordingly, it is the primary object of the present invention to provide a method for fabricating a bit line contact between two adjacent gate conductor stacks by utilizing a sacrificial polysilicon layer and spin-on glass (SOG) during the fabrication of a Trench-DRAM device, thereby solving the above-described problems.

[0011] According to the claimed in invention, a method for fabricating a bit line contact hole is provided. A substrate having a main surface is prepared. At least two adjacent gate conductor stacks are provided on the main surface. A bit line contact area and a non-bit line contact area are defined over the main surface. The bit line contact area is directly above an area between the two adjacent gate con-

ductor stacks. Each of the gate conductor stacks has a top surface and sidewalls. A silicon oxide liner is deposited on the top surface and sidewalls of each of the gate conductor stacks. A sacrificial layer is thereafter deposited on the silicon oxide liner. A first chemical mechanical polishing (CMP) is carried out to polish the sacrificial layer. A spin-on-glass (SOG) layer is then coated onto the remaining sacrificial layer and onto the exposed top surface of the gate conductor stacks. A photoresist pattern is formed on the SOG layer masking the bit line contact area. Using the photoresist pattern as a hard mask, the SOG layer, the sacrificial layer, and the silicon oxide liner not covered by the photoresist pattern is etched away. The photoresist pattern is then removed, leaving the SOG layer, the sacrificial layer, and the silicon oxide liner within the bit line contact area intact. A silicon nitride liner is deposited on the SOG layer within the bit line contact area, the partial top surface and sidewalls of the gate conductor stacks. A dielectric layer is then deposited over the silicon nitride liner. A second CMP is performed to polish the dielectric layer to stop on the SOG layer. The remaining SOG layer and the sacrificial layer within the bit line contact area are selectively removed to form the bit line contact hole.

[0012] Other objects, advantages, and novel features of the claimed invention will become more clearly and readily apparent from the following detailed description when taken in conjunction with the accompanying drawings.

Brief Description of Drawings

[0013] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention. In the drawings:

[0014] Fig.1 to Fig.5 are schematic cross-sectional diagrams illustrating a conventional method for fabricating a bit line contact between two adjacent gate conductor stacks; and

[0015] Fig.6 to Fig.13 are schematic cross-sectional diagrams showing a method for fabricating a bit line contact between two adjacent gate conductor stacks by utilizing a sacrificial polysilicon layer and spin-on glass (SOG) during the fabrication of a Trench-DRAM device in accordance with one preferred embodiment of the present invention.

Detailed Description

[0016] Please refer to Fig.6 to Fig.13. Fig.6 to Fig.13 are

schematic cross-sectional diagrams showing a method for fabricating a bit line contact between two adjacent gate conductor stacks by utilizing a sacrificial polysilicon layer and spin-on glass (SOG) during the fabrication of a Trench-DRAM device in accordance with one preferred embodiment of the present invention, wherein like numerals designate similar regions, layers or elements.

[0017] As shown in Fig.6, at least two adjacent gate conductor (GC) stacks 12 and 14 are formed on a main surface 11 of a semiconductor substrate 10. Each of the gate conductor stacks 12 and 14 generally comprises a gate dielectric layer 22, a conductive layer 24 and a silicon nitride cap layer 26. The conductive layer 24 may be made of metals or metal silicide alloys. According to this invention, each of the gate conductor stacks 12 and 14 is about 5000-angstrom height. The silicon nitride cap layer 26 is about 2000-angstrom thick. A bit line contact area 42 and a non-bit line contact area 44 are defined over the gate conductor stacks 12 and 14. The bit line contact area 42 is approximately above the area between the gate conductor stacks 12 and 14. According to this invention, the dimension of the bit line contact area 42 is about 90nm.

[0018] After forming the gate conductor stacks 12 and 14, a

chemical vapor deposition (CVD) process is carried out to deposit a silicon dioxide liner 102 over the semiconductor substrate 10. The silicon dioxide liner 102 covers sidewalls and top surface of the gate conductor stacks 12 and 14. Subsequently, a sacrificial polysilicon layer 104 having a thickness of about 4000 angstroms is deposited on the silicon dioxide liner 102.

[0019] As shown in Fig.7, a first CMP process is performed to polish the sacrificial polysilicon layer 104 down to the silicon nitride cap layer 26 of the gate conductor stacks 12 and 14. By doing this, a precise end point detection can be obtained because the silicon nitride cap layer 26 of the gate conductor stacks 12 and 14 is used as polishing stop layer during the first CMP process. An optional over-etching may be performed. Another unexpected advantage of using the silicon nitride cap layer 26 of the gate conductor stacks 12 and 14 as polishing stop layer is that an alignment mark (not shown) made of the same layer as the silicon nitride cap layer 26 is also exposed, thus providing precise alignment of the wafer without the fear of interference of the polysilicon layer. The alignment mark fabricated on scribe lines or peripheral areas of a die or a chip is known in the art. It is noteworthy that after the

first CMP, as specifically indicated in Fig.7, dishing phenomenon on the sacrificial polysilicon layer 104 may be observed within the non-bit line contact area 44.

[0020] As shown in Fig.8, a layer of spin-on glass (SOG) 106 is coated on the semiconductor substrate 10. The SOG layer 106 has a thickness of about 3000 angstroms and covers the silicon nitride cap layer 26 of the gate conductor stacks 12 and 14, the remaining sacrificial polysilicon layer 104, and the exposed silicon dioxide liner 102. A photoresist pattern 108 is then formed on the SOG layer 106 by using conventional lithographic methods. The photoresist pattern 108 masks the bit line contact area 42 directly above the area between the two adjacent gate conductor stacks 12 and 14, while the non-bit line contact area 44 is exposed. It is advantageous to use the present invention method because the SOG layer 106 provides uniform and planar surface for the photoresist pattern 108. Besides, the SOG layer 106 compensates the slightly recessed dishing area over the sacrificial polysilicon layer 104 in the non-bit line contact area 44.

[0021] As shown in Fig.9, using the photoresist pattern 108 and the silicon nitride cap layer 26 together as an etching hard mask, a conventional dry etching process is carried out to

etch away the SOG layer 106, the sacrificial polysilicon layer 104, and silicon dioxide liner 102, which are not masked by the photoresist pattern 108, leaving the SOG layer 106, the sacrificial polysilicon layer 104 and silicon dioxide liner 102 within the bit line contact area 42 intact. The photoresist pattern 108 is then removed.

[0022] As shown in Fig.10, a thin silicon nitride liner 110 is then deposited on the semiconductor substrate 10 by CVD methods. The thin silicon nitride liner 110 covers the exposed main surface 11 of the substrate 10, a part of the top surface and sidewalls of the gate conductor stacks 12 and 14, and the remaining SOG layer 106. A CVD process is performed to deposit a borophosphosilicate glass (BPSG) layer 120 over the thin silicon nitride liner 110. The BPSG layer 120 has a thickness of about 4000~8000 angstroms.

[0023] As shown in Fig.11, a second CMP is carried out to polish the BPSG layer 120. The second CMP is terminated when the SOG layer 106 is exposed. It is noted that the thin silicon nitride liner 110 within the bit line contact area 42 is removed.

[0024] As shown in Fig.12, the remaining SOG layer 106 and the sacrificial polysilicon layer 104 are selectively removed

from the bit line contact area 42 so as to form a bit line contact hole 130.

[0025] As shown in Fig.13, subsequently, an anisotropic dry etching process is performed to etch the silicon dioxide liner 102, thereby exposing the silicon main surface 11 within the bit line contact hole 130 and forming silicon dioxide spacers 142 on sidewalls of the gate conductor stacks 12 and 14. Finally, the bit line contact hole 130 is filled with conductive materials such as metals or the like to form a bit line contact plug 150.

[0026] Those skilled in the art will readily observe that numerous modifications and alterations of the present invention method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.